REMARKS

Present Status of the Application

The Office Action mailed on September 22nd, 2004 rejected claims 9-12 and 15-18 under 35 U.S.C. 103(a), as being unpatentable over Chang et al. (U.S. 6,754,105) in view of Hwang (U.S. 6,699,757). The Office Action also indicated that claims 13 and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants appreciate this indication of allowable subject matter. Applicants have amended claim 9 to improve clarity and no new matter has been added to the application by the amendments made herein. After entry of the foregoing amendments, claims 9-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Summary of Applicant's Invention

The Applicant's invention is directed to a non-volatile memory device having a gate formed in a trench in a substrate. In the non-volatile memory device provided by the invention, the source/drain regions are located at **both sides of the trench in the substrate near the surface of the substrate.** Besides, charge-trapping layer **not only is located at the sidewall of the trench but also is located at the bottom of the trench.** Because the gate is fabricated within a trench in this invention, the coupling ratio of the device can be increased under the same device dimension so that the storage efficiency of

the memory device is improved. Furthermore, depth of the trench is adjustable so that more charges can be stored inside the non-volatile memory device. In other words, the threshold voltage (V_t) for programming data can be changed by adjusting the depth of the trench.

Discussion of Office Action Rejections

The Office Action rejected the claims 9-12 and 15-18 under 35 U.S.C. 103(a), as being unpatentable over Chang et al. (U.S. 6,754,105) in view of Hwang (U.S. 6,699,757) and stated that

> *Chang et al disclose most of the feature claimed in claims 9-12 and 15-18 except mention the requirement of plurality of source/drain diffusion regions. However, Hwang discloses a method for manufacturing embedded non-volatile memory with sacrificial layers.....*

Applicants respectfully traverse this rejection but have amended claim 9 to clearly define the method according to the invention. As amended, claim 9 recites:

> *Claim 9. (currently amended) A non-volatile memory device, comprising:*
> *a substrate, wherein the substrate has a trench;*
> *a gate disposed over and completely filling the trench;*
> *a bottom oxide layer disposed between the gate and the trench surface;*
> *a charge-trapping layer disposed between the gate and the bottom oxide layer;*
> *a top oxide layer disposed between the gate and the charge-trapping layer; and*
> *a plurality of source/drain regions **located at both sides of the trench in the substrate**.*

(*Emphasis Added*). Applicants submit that the claims patentably define over the prior art of record, for at least the reason that the prior arts fail to disclose at least these elements emphasized above.

Applicants emphasize that in the present invention, the source/drain regions are located at both sides of the trench in the substrate near the surface of the substrate. Further, the charge-trapping layer is located not only at the sidewall of the trench but also at the bottom of the trench. Because of the large coverage area, the number of charges trapped by the charge-trapping layer is high.

Chang et al. disclose a flash memory device having a select gate 66a/66b formed in the substrate. In the cited reference provided by Chang et al., the charge-trapping region 50 is located at the sidewall of the select gate. Chang et al. further emphasize that "each memory device 42 includes a complimentary pair of charge trapping regions 50a and 50b.....each memory device 42 can be considered a dual cell, non-volatile, flash electrically erasable and programmable memory device 42." (column 4, lines 45-52). Therefore, it is clear that the charge trapping regions 50 in the cited prior art are formed on the sidewall of the select gate and are separated from each other so as to form a dual charge storage cell for a bi-direction flash memory operation controlled by the select gate. Furthermore, Chang et al. also fail to teach or suggest that the charge trapping region can be formed to cover the surface of the trench. Since the charge trapping region is located at a portion of the surface of the select gate mentioned by Chang et al., the number of the charges trapped by the charge trapping region is much less than the

number of the charges trapped by the charge trapping layer formed to cover the surface of the trench. Further, Chang et al. also fail to teach or mention that the source/drain region can be formed at both sides of the trench near the surface of the substrate. On the other hand, Change et al. emphasize the formation of the bit lines 62a and 62b at the bottom of the select gate 66a/66b as an electron emitter or receiver during the read/write operation of the flash memory. In the view of operating the flash memory, it is obvious that the existence of the bit line 62a and 62b is necessary and the location of the bit line 62a and 62b is a main feature of the cited art. Although Hwang mention the formation of the source/drain regions 147/148 in the substrate, there is no motivation to combine these two cited arts since Chang et al. fails to teach or suggest the formation of the source/drain regions. Even though the people skilled in the art combined the cited arts, the combination result would not possess the features and the advantages the same as those of the present invention. Therefore, Claim 9 is believed to be patentably distinguished over the cited arts according to at least reasons described and discussed above, so that reconsideration and withdrawal of the Office Action's rejections are respectfully requested.

However, claims 10-18 respectively depend from claim 9. Claims 10-18 are submitted to be patentably distinguishable over the cited references for at least the same reasons as independent claim 9, from which these claims respectively depend, as well as for the additional features that these claims recite.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 9-18 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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